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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,961	08/20/2003	Chun Ho Fan	50626.53	4980

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EXAMINER	
BEREZNY, NEMA O	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,961	FAN ET AL.	
	Examiner	Art Unit	
	Nema O. Berezny	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23 and 30-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23 and 30-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2-15-05 has been entered. Claims 1-23 and 30-35 are currently pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 8-17, and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (2002/0180035) in view of Weber (5,609,889). Huang discloses a process for manufacturing a plurality of integrated circuit packages comprising: mounting a plurality of semiconductor dice (Figs.2A-2G; Fig.4 el.41) to a first surface (el.400) of a substrate array (el.40); mounting a plurality of die adapters (el.48) to said semiconductor dice such that each one of said die adapters is mounted to a corresponding one of said semiconductor dice; wire bonding (el.42) said

semiconductor dice to ones of conductive traces located on said first surface (p.4 para.43) of said substrate array (Fig.4); mounting a plurality of collapsible spacers (el.46) to one of a heat spreader array (el.43), said die adapters, and said substrate array; placing one of said heat spreader array and said substrate array in a mold cavity (Fig.2E; p.3 para.36); releasably clamping the other of said heat spreader array and said substrate array to a first die of said mold such that said collapsible spacers are disposed between said heat spreader array and said substrate array (Fig.4; p.3 para.36); molding (el.44) the semiconductor dice, said substrate array, said wire bonds, said die adapters, said collapsible spacer array and said heat spreader array into a molding compound by molding in a mold cavity between said other of said heat spreader array and said substrate array and said surface of the lower mold die resulting in an array of molded packages having at least a portion of said substrate array exposed and at least a portion of said heat spreader array exposed from said array of molded packages(Fig.4); forming a plurality of ball grid arrays (el.49) on a second surface (el.401) of said substrate array, bumps (el.49) of said ball grid arrays being electrically connected to said conductive traces (p.4 para.43); and singulating each integrated circuit package from said array of molded packages (Fig.2G; p.3 para.38). However, Huang does not disclose placing one of said heat spreader array and said substrate array on a surface of a lower mold die, and releasably clamping the other of said heat spreader array and said substrate array to an upper mold die. Huang would look to one such as Weber for preventing molding from covering the bottom surface of the substrate array because Weber discloses placing one of said heat spreader and

said substrate (Figs.3,5 el.5,6,7) on a surface of a lower mold die (el.23') wherein said placing comprises placing said substrate in said mold cavity such that said substrate rests on said surface of said lower mold die (Fig.5), releasably clamping (el.39) the other of said heat spreader (el.19) and said substrate to an upper mold die (el.22) wherein said releasably clamping comprises releasably clamping said heat spreader to said upper mold die, such that said other of said heat spreader and said substrate is in contact with said upper mold die (col.6 line 66 – col.7 line 1); molding the semiconductor die (el.20), the substrate, the wire bonds (el.21,21A), and said heat spreader into a molding compound (el.35) by molding in a mold cavity (el.27) between said other of said heat spreader and said substrate and said surface of the lower mold die resulting in a molded package having at least a portion of said substrate exposed and at least a portion of said heat spreader exposed from said molded package (Fig.3). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the mold die of Weber with the process of Huang in order to prevent molding material from covering the lower surface of the substrate (Weber - col.7 lines 1-7) **[claims 1, 4, 5, 13, 16, 17].**

Based upon the rejection of claims 1 and 13 above, Weber also discloses wherein said placing one of said heat spreader array and said substrate array in a mold cavity comprises placing said heat spreader array in said mold cavity such that said heat spreader array rests on said surface of said lower mold die (col.5 lines 52-61). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the upper and lower mold dies of Weber with the process of

Huang to allow flexibility in making the dies interchangeable (Weber – col.5 lines 52-61) **[claims 2, 14]**.

Based upon the rejection of claims 1 and 13 above, Weber also discloses wherein said releasably clamping comprises releasably clamping said substrate array to said upper mold die (col.5 lines 52-61). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the upper and lower mold dies of Weber with the process of Huang to allow flexibility in making the dies interchangeable (Weber – col.5 lines 52-61) **[claims 3, 15]**.

Based upon the rejection of claims 1 and 13 above, Huang also discloses wherein said mounting said collapsible spacers comprises mounting said collapsible spacer array (el.45) to said substrate array (Fig.4) **[claims 8, 20]**; wherein said mounting said collapsible spacer array comprises mounting said collapsible spacer array (el.46) to said heat spreader array (Fig.4) **[claims 9, 21]**; wherein mounting said collapsible spacers further comprises mounting a corresponding collapsible spacer of said collapsible spacer array to each of said plurality of die adapters (Fig.4 el.47) **[claim 22]**; wherein said at least one collapsible spacer comprises a plurality of collapsible spacers, and mounting said at least one collapsible spacer comprises mounting one of said plurality of collapsible spacers (el.47) to said die adapter and mounting at least another of said collapsible spacers (el.45) to said substrate (Fig.4) **[claim 10]**; and wherein said collapsible spacers (el.46) are disposed between said die adapter and said heat spreader and in contact with said die adapter and said heat spreader during molding (Fig.4) **[claims 11, 12, 23]**.

Claims 6 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang in view of Weber as applied to claims 1 and 13 above, and further in view of Punzalan et al. (200310160309). Huang and Weber do not disclose a ground wire bonding said die to said adapter. However, Huang and Weber would look to one such as Punzalan for a separate ground attachment from the die attach area because Punzalan discloses wherein said bonding further comprises ground wire bonding (Fig.4 el.27) a die adapter(s) (el.54) to a corresponding semiconductor die/dice (el.12). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the ground wire bonding of Punzalan with the process of Huang and Weber in order to provide a ground plane to a semiconductor structure separate from the die attach area (Punzalan - p.4 para.86).

Claims 7 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang in view of Weber as applied to claims 1 and 13 above, and further in view of Cheng et al. (2003/0075812). Huang and Weber do not disclose ground wire bonding said die to said substrate. However, Huang and Weber would look to one such as Cheng for reducing inductance because Cheng discloses wherein wire bonding further comprises ground wire bonding (Fig.7 el.21a) a semiconductor die/dice (el.10) to a corresponding ground pad (el.30) on a substrate array (el.12). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use

the ground wire bonding of Cheng with the process of Huang and Weber in order to reduce the inductance effect (Cheng - p.3 para.42).

Claims 30 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang in view of Weber as applied to claims 1 and 13 above, and further in view of Mayer (2003/0226253). Huang in view of Weber do not disclose a collapsible spacer comprising a solder perform. However, Huang and Weber would look to one such as Mayer for surface conformity because Mayer discloses wherein said mounting at least one collapsible spacer comprises mounting a solder preform (Fig.5A el.20) to at least one of said heat spreader (el.52), said die adapter and said substrate (p.3 para.27). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the solder preform of Mayer with the process of Huang and Weber in order to provide better conformity to the surfaces to be bonded (Mayer - p.1 para.4).

Claims 31-32 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang in view of Weber as applied to claims 1 and 13 above, and further in view of Fang (2003/0189245). Huang in view of Weber do not disclose a collapsible spacer comprising spherical collapsible balls. However, Huang and Weber would look to one such as Fang for an adhesive and thermal conductor because Fang discloses wherein said mounting at least one collapsible spacer comprises mounting substantially spherical collapsible solder balls (Fig.3 el.308) to at least one of said heat

spreader (el.306), said die adapter and said substrate. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the solder balls of Fang with the process of Huang and Weber in order to provide a conductor that functions as both an adhesive and a thermal conductor.

Response to Arguments

Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nema O. Berezny whose telephone number is (571) 272-1686. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NB

Laura M Schultz